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(54) Monolithic ADSL analogue front end

(57) A monolithic ADSL analog front end 500 implements mixed signal technology in which synthesized impedance techniques are employed. The synthesized impedance techniques substantially reduce the transmitter line driver 506 gain and receiver amplifier 508 gain such that the analog transmitter and receiver filters 502, 504 can be implemented in the high-voltage process. Since the signal gains of the transmitter line driver 506 and receiver amplifier 508 are reduced, and since the analog filters 502, 504 are implemented in the high-voltage process, they can be physically reduced in size to accommodate a higher noise floor which reduces the die area and power dissipation requirements associated with the hybrid 500.

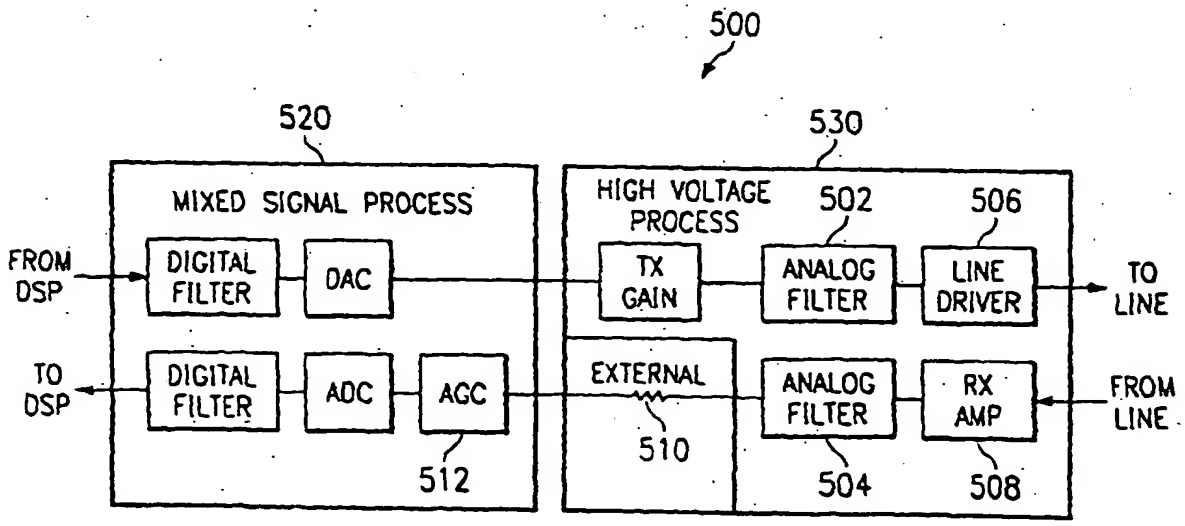

FIG. 5

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Description

Technical Field of the Invention

[0001] This invention relates generally to asymmetric digital subscriber lines (ADSL), and more particularly to a monolithic ADSL analog front end.

Description of the Prior Art

[0002] Asymmetric digital subscriber lines (ADSL) can supply the necessary bandwidth for applications such as fast access to the Internet, video conferencing, interactive multimedia, and Video-on-Demand. This technology is designed to solve the most severe bottleneck in the data access network between the Central Office and the customer, or end-user.

[0003] ADSL is a new modem technology that converts existing copper telephone lines into access paths for multimedia and high-speed data communications, and maintains the regular telephone voice services. ADSL provides data rates that expand the best existing access capacity (i.e., ISDN) by a factor of 60 or more, and the best existing common analog access capacity (i.e., V.34 modems) by a factor of 300, without requiring any new cabling. ADSL can practically transform the existing public information network from one limited to voice, text and low resolution graphics to a powerful, ubiquitous system capable of carrying multimedia, including full motion video, to everyone's home.

[0004] Rate adaptive ADSL delivers any data rate from 64kbps to 8.192Mbps on the downstream channels to the subscribers and any data rates from 16kbps to 768kbps on the upstream channels back to the network, while simultaneously providing lifeline POTS (Plain Old Telephone Service), all over a single twisted copper wire pair. The downstream and upstream channels can be split into several sub-channels (up to 4 sub-channels on the downstream and 3 bi-directional sub-channels) to serve several applications simultaneously.

[0005] The ADSL operates over a single, unconditioned twisted copper pair of wires. Its connection is via modem pairs, one at the user end and the second at the Central Office.

[0006] A common strategy for implementing ADSL modem technology is to ensure that the input impedance of an analog front end (AFE), looking into the subscriber loop port, matches the loop characteristic impedance. This has traditionally been accomplished by placing a network that closely matches the loop characteristic impedance between the AFE line driver output and the subscriber loop (or transformer coupling to the subscriber loop). A single-ended version of this scheme is shown in Figure 1. A disadvantage associated with such schemes is that half of the line driver output signal power is dissipated on this terminating network.

[0007] Another problem associated with the AFE concerns IC fabrication processes that are generally optimized for mixed signal circuits, and are not therefore compatible with the large voltage swings encountered on the subscriber loop. A common way to remedy this problem is to implement virtually all of the required data conversion and filter functions on the low voltage process and then amplify or attenuate the signal as required to connect to the subscriber line using a high-voltage analog process technology such as shown in Figure 2. Circuits implemented in the low voltage process must have very low noise. They are therefore large and consume excessive power to eliminate the undesirable noise.

[0008] In view of the foregoing, a need exists for an ADSL analog front end that uses less power than known asymmetric digital subscriber loop AFE architectures.

Summary of the Invention

[0009] The present invention is directed to synthesized impedance AFE IC for ADSL applications and that includes the transmitter line driver, receiver and analog transmitter and receiver filters implemented in a common high voltage process. The AFE is partitioned in such a way that allows a reduction in die area and power dissipation of the analog filters over known AFE architectures that implement the analog filters in a low voltage process in order to reduce noise generated in the filters. The present AFE uses synthesized impedance to implement the transmitter line driver. This reduces the power dissipation of the line driver. The active current sensing impedance associated with the line driver is importantly scaled which results in less power wasted on the loop current sensing resistor for a given loop current. This effectively lowers the line driver output voltage and translates to a reduction in the line driver power supply voltage resulting in a substantially reduced line driver noise gain. Since the line driver noise gain is substantially reduced, the AFE analog filters can be implemented along with the line driver in the high voltage process instead of the more conventional low voltage process commonly employed in the prior art. This allows the analog filters to employ smaller filtering components having a higher noise floor, since the filter noise is no longer substantially amplified by the line driver.

[0010] In one aspect of the invention, a monolithic ADSL analog front end is implemented that has the line driver, receiver and analog transmitter and receiver filters implemented in a high voltage process.

[0011] In another aspect of the invention, a monolithic ADSL analog front end is implemented using an active termination circuit to synthesize the line driver source impedance.

[0012] In yet another aspect of the invention, a monolithic ADSL analog front end is implemented to substantially reduce die area and power dissipation associated with the analog filters.

[0013] In still another aspect of the invention, a monolithic ADSL analog front end is implemented such that

noise generated by the transmitter analog filter is not amplified.

[0014] In still another aspect of the invention, a monolithic ADSL analog front end has a receiver analog filter implemented in a high voltage process allowing an increase in the noise floor to reduce power dissipation and die area requirements.

Brief Description of the Drawings

[0015] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following detailed description of certain particular and illustrative embodiments and the features and aspects thereof, by way of example only, and with reference to the figures of the accompanying drawings in which:

Figure 1 is a schematic diagram illustrating a traditional passively terminated line driver circuit;
Figure 2 illustrates a common technology strategy for implementing an ADSL analog front end;
Figure 3 is a schematic diagram illustrating an active termination line driver circuit;
Figure 4 is a schematic diagram illustrating a receiver amplifier circuit using passive elements around the receive amplifier to achieve high 4-wire echo return loss;
Figure 5 is a functional diagram illustrating an ADSL analog front end that has been repartitioned according to an embodiment of the present invention; and
Figure 6 is a block diagram illustrating an analog front end circuit that is partitioned according to the inventive principles presented herein according to an embodiment of the present invention.

[0016] While the above-identified drawing figures set forth particular embodiments, other embodiments of the present invention are also contemplated, as noted in the following discussion. In all cases, this disclosure presents illustrated embodiments of the present invention by way of representation and not limitation. Numerous other modifications and embodiments can be devised by those skilled in the art which fall within the scope and spirit of the principles of this invention.

Detailed Description of the Preferred Embodiments

[0017] Figure 1 is a schematic diagram illustrating a traditional passively terminated line driver circuit 100. Such passively terminated line driver circuits 100 have traditionally been employed in hybrid circuits used to interface the four-wire signal path (two wires each from DAC and to ADC) to the bi-directional two-wire path (subscriber loop). The line driver circuit 100 ensures that the input impedance of the hybrid, looking into the subscriber loop port, matches the loop characteristic impedance. This line driver circuit 100 undesirably causes half of the line driver output signal power to be dissipated in the terminating network.

[0018] Figure 2 illustrates a common technology strategy for implementing an ADSL analog front end (AFE) 200. The AFE 200 architecture is not optimised for mixed signal circuits that are incompatible with the large voltage swings encountered on the subscriber loop. Instead, all of the required data conversion and analog filter 202, 204 functions are implemented on the low-voltage mixed signal process 206. Signals are amplified or attenuated as required to connect the AFE 200 to the subscriber line using a high-voltage analog process technology 208. This architecture is undesirable for ADSL applications since circuits implemented in the low-voltage technology 206 must have very low noise, and therefore are large and consume excessive power.

[0019] Figure 3 is a schematic diagram illustrating an active termination line driver circuit 300. The line driver circuit 300 demonstrates a single-ended technique for achieving impedance matching to the subscriber loop using synthesized impedance. Node B 302 represents the end of the subscriber loop (or equivalently, the input to the loop-coupling transformer, not shown), where the impedance of the subscriber loop is represented by R_L 304. The amplifier 306 with gain, G, amplifies the voltage drop across the loop current sensing resistor, R_S 308. Because R_T 310 >> R_S 308, the equal resistors R_T 310 and the high gain of the line driver amplifier 306 forces $V_B = 2V_T - V_S = 2V_T - GR_S I$, where I represent the loop current. The termination impedance is expressed as $Z_{IN} = -dV_B/dI = GR_S$, and the loop impedance matching condition is $GR_S = R_L$ 304. The feedback network in the active termination circuit 300 therefore creates an effective termination equal to the current sense resistance, R_S 308, multiplied by the feedback amplifier 306 gain.

[0020] Scaling the terminating impedance is important because for a given loop current, less power is wasted on resistor, R_S 308. This means that the line driver output voltage is lower. When $V_R = 0$, in order to deliver signal V_T to the loop, the traditional line driver 100 shown in Figure 1 must provide $2V_T$, whereas only $V_T(1+G^{-1})$ is required of the actively terminated line driver 300. Thus, the power wasted in the termination network (R_S) is reduced by a factor of G. This translates to a reduction in the line driver power supply voltage and consequently a reduction in the power consumed by the line driver. The present inventors recognized the important ramifications that the foregoing described characteristics have on process technology choices regarding a monolithic ADSL analog font end that includes a line driver, receiver and analog transmitter and receiver filters discussed herein below with reference to Figure 5.

[0021] The foregoing argument for impedance synthesis is certainly valid for small V_R, but there are environments where the receiver signal, V_R, is not negligible, such as for example, on short subscriber loops. A power reduction procedure is fortunately prescribed for

short loops. Consequently, where the receiver power is high, the transmitter power is reduced. The maximum signal that the line driver amplifier 306 is only slightly greater than $V_T(1+G^{-1})$, so a substantial reduction in line driver power supply voltage and power consumption is obtained.

[0022] A monolithic ADSL analog front end used to interface the four-wire signal path to the bi-directional two-wire path is required to have low 4-wire (tx) to 2-wire insertion loss, low 2-wire to 4-wire (rx) insertion loss, high 4-wire (tx) to 4-wire (rx) echo return loss, and high 2-wire echo return loss. High 2-wire echo return loss is achieved when the effective driver impedance is matched to the loop impedance. High 4-wire echo return loss requires a hybrid circuit that forms the linear combination of V_A and V_B such that the portion of the signal due to V_T is eliminated. When either the passively or actively terminated drivers are employed, the correct linear combination is $V_{RX} = G_{RX}((R_L{}^*V_A)/(R_S + R_L) - V_B) = -2G_{RX}R_S/(R_S + R_L)$, where G_{RX} represents the receiver amplifier gain. Since R_S is G times smaller when active termination is employed, G_{RX} used for active termination must be G times that used for passive termination to produce the same V_{RX}. This requirement was found by the present inventors to be the only apparent disadvantage of active termination, since it means that the receiver amplifier input-referred noise must be G times lower in order to provide the same receiver dynamic range as achieved with a passively terminated driver.

[0023] Figure 4 is a schematic diagram illustrating a receiver amplifier circuit 400 using passive elements around the receive amplifier to achieve high 4-wire echo return loss. The amplifier circuit 400 is an alternative to the traditional hybrid circuit. The amplifier circuit 400 realizes the echo return loss linear combination using the passive elements around the receive amplifier to enable a reduction in the number of passive components.

[0024] The present inventors recognized that the features described herein above could be implemented to realize a monolithic ADSL analog front end (AFE) functional architecture that is partitioned to provide a hybrid that requires substantially less die area and power dissipation than known architectures using mixed signal circuits such as shown in Figure 2. Figure 5 is a functional block diagram illustrating an ADSL analog front end 500 that has been repartitioned according to one embodiment of the present invention in order to minimize power dissipation and to minimize IC die area requirements. The foregoing repartitioning can be seen to be implemented using functional blocks, including analog transmitter and receive filters 502, 504, a transmitter line driver 506 and a receiver amplifier 508. When the line driver 506 is implemented using synthesized impedance techniques as described above, the line driver 506 gain is substantially reduced such that a substantial reduction is noise gain is also achieved (in some schemes, the line driver gain can be nominally 0dB). The noise contributed by the transmitter analog filter 502 is therefore not amplified. This feature allows the transmitter analog filter 502 to be repartitioned differently than that required by traditional partitioning, since the noise floor of the transmitter analog filter 502 can now be higher. Since the noise floor can be higher, smaller components can be used to implement the filter 502, with a resulting reduction in hybrid die area and power dissipation. A similar argument applies to the receive analog filter 504. According to one embodiment, moving the receive analog filter 504 to the high voltage process was fount to allow an increase in its noise floor of approximately 17.5dB. As stated herein before, the traditional approach disclosed in the prior art partitions the functions such that virtually all of the required data conversion and filter functions are implemented on the low-voltage process. Signals are then amplified or attenuated as required to connect to the subscriber line using a high-voltage analog process technology. The familiar approach used in the prior art requires circuits that are large and that consume undesirably excessive amounts of power in order to eliminate noise that caused by implementing the circuits on the low-voltage process. Looking again at Figure 5, an external resistor 510 forms part of the variable gain amplifier portion of the AGC 512 and operates to isolate the mixed signal process 520 from the high voltage process 530. According to one embodiment, the AGC 512 setting is chosen such that its output is as close as possible to 3Vpp to implement the ADSL analog front end 500 using a BiCOM 2 process.

[0025] Figure 6 is a block diagram illustrating a realizable analog front end circuit (AFE) 600 that is partitioned according to the inventive principles presented herein above. The AFE 600 can be seen to include line driver 602, receiver amplifier 604, analog receive filter 608, analog transmitter filter 610 and transmitter gain circuit 610.

[0026] In view of the above, it can be seen the present invention presents a significant advancement in the art of ADSL analog front end technology. Further, this invention has been described in considerable detail in order to provide those skilled in the data communication art with the information needed to apply the novel principles and to construct and use such specialized components as are required. In view of the foregoing descriptions, it should further be apparent that the present invention represents a significant departure from the prior art in construction and operation. However, while particular embodiments of the present invention have been described herein in detail, it is to be understood that various alterations, modifications and substitutions can be made therein without departing in any way from the spirit and scope of the present invention. For example, although various embodiments have been presented herein with reference to particular functional architectures and characteristics, the present inventive structures and characteristics are not necessarily limited to particular circuit architectures or sets of characteristics as used herein. It shall be understood the embodiments

described herein above can easily be implemented using many diverse signal processing elements so long as the combinations achieve a monolithic ADSL analog front end according to the inventive principles set forth herein above.

Claims

1. A hybrid ADSL analog front end comprising:

   low-voltage mixed signal processing means for digitally filtering and converting a digital host signal to an analog host signal and further for digitally filtering and converting an analog subscriber loop signal to a digital subscriber loop signal; and
   high-voltage processing means for filtering the analog host signal and synthesizing a subscriber loop input impedance through which the filtered analog host signal can be transmitted to a subscriber loop and further for amplifying and filtering an analog signal received via the subscriber loop to generate the analog subscriber loop signal.

2. The hybrid ADSL analog front end according to claim 1 wherein the high-voltage processing means for filtering the analog host signal comprises an analog filter.

3. The hybrid ADSL analog front end according to claim 2 wherein the high-voltage processing means for filtering the analog signal received via the subscriber loop comprises an analog filter.

4. The hybrid ADSL analog front end according to claim 1 further comprising means for isolating the low-voltage mixed signal processing means from the high-voltage processing means.

5. The hybrid ADSL analog front end according to claim 4 wherein the isolating means comprises an external resistor.

6. The hybrid ADSL analog front end according to claiml 1 wherein the high-voltage processing means for synthesizing a subscriber loop input impedance comprises an active termination line driver circuit.

7. The hybrid ADSL analog front end according to claim 1 wherein the high-voltage processing means for amplifying an analog signal received via the subscriber loop comprises a plurality of impedances and a differential amplifier in combination and operational to achieve a high 4-wire echo return loss associated with a predetermined subscriber loop signal.

8. An ADSL analog front end comprising:

   a low-voltage mixed signal process comprising a digital-to-analog converter (DAC), an analog-to-digital converter (ADC), an input digital filter, an output digital filter and an automatic gain control (AGC), wherein the input digital filter is operational to filter input signals received by the DAC, the output digital filter is operational to filter output signals generated by the ADC, and the AGC is operational in response to an amplified and filtered received subscriber loop signal to generate an analog signal input to the ADC having a predetermined peak-to-peak value; and
   a high-voltage process comprising a transmitter gain portion, a transmitter analog filter, a transmitter line driver, a receiver amplifier and a receive analog filter, wherein the transmitter gain portion is operational to amplify an analog signal generated by the DAC, the transmitter analog filter is operational to filter a signal generated by the transmitter gain portion to generate a filtered transmitter signal therefrom, the transmitter line driver is operational to amplify or attenuate the filtered transmitter signal to achieve a desired ADSL characteristic, the receive amplifier is operational to receive a subscriber loop signal to generate an amplified received subscriber loop signal therefrom, the receive analog filter is operational to filter the amplified received subscriber loop signal to generate the amplified and filtered received subscriber loop signal.

9. The ADSL analog front end according to claim 8 further comprising an external isolation resistor operational to isolate the low-voltage mixed signal process from the high-voltage process.

10. The ADSL analog front end according to claim 8 wherein the transmitter line driver comprises an active termination line driver circuit.

11. The ADSL analog front end according to claim 8 wherein the receiver amplifier comprises a plurality of passive impedance elements and a differential amplifier configured to achieve a high 4-wire echo return loss associated with the subscriber loop.

12. A monolithic ADSL analog front end comprising:

   a low-voltage mixed signal portion including a first digital filter having an input and an output, a DAC having an output and an input in communication with the first digital filter output, a

second digital filter having an input and an output, an ADC having input and an output in communication with the second digital filter input, and an AGC having an input and an output in communication with the ADC input; and
a high-voltage portion including a transmitter gain element having an output and an input in communication with the DAC output, a first analog filter having an output and an input in communication with the transmitter gain element output, a line driver having an output and an input in communication with the first analog filter output, a receive amplifier having an input and an output, and a second analog filter having an output in communication with the AGC input and an input in communication with the receive amplifier output.

13. The monolithic ADSL analog front end according to claim 12 wherein the AGC comprises an external resistor that is operational to isolate the low-voltage mixed signal portion from the high-voltage portion.

14. The monolithic ADSL analog front end according to claim 12 wherein the line driver comprises an active termination circuit.

15. The monolithic ADSL analog front end according to claim 12 wherein the receive amplifier comprises a plurality of passive impedance elements and a differential amplifier configured to achieve a high 4-wire echo return loss associated with a predetermined subscriber loop.

16. A method of achieving a high 4-wire echo return loss associated with a monolithic ADSL analog front end configured to interface a four-wire signal path to a bi-directional two-wire subscriber loop comprising the steps of:

digitally filtering a digital input signal via a low-voltage mixed signal process to generate a digitally filtered input signal;
converting via the low-voltage mixed signal process, the digitally filtered input signal to an analog signal;
amplifying the analog signal via a high-voltage process to generate an amplified analog signal;
analog filtering the amplified analog signal via an analog filter implemented in the high-voltage process;
synthesizing in the high-voltage process a desired ADSL input impedance; and
transmitting the amplified and analog filtered analog signal to predetermined ADSL via the synthesized ADSL input impedance.

17. The method according to claim 16 further comprising the step of amplifying via a high-voltage process impedance synthesizer, an input signal received from a predetermined ADSL to generate a signal having a high 4-wire echo return loss.

18. The method according to claim 17 further comprising the step of analog filtering in the high-voltage process, the signal having a high 4-wire echo return loss.

19. A method according to claim 18 further comprising the step of communicating the filtered signal having a high 4-wire echo return loss to the low-voltage mixed signal process via an isolation element.

20. The method according to claim 19 further comprising the step of amplifying in the low-voltage mixed signal process, the filtered signal having a high 4-wire echo return loss.

21. The method according to claim 20 further comprising the step converting to a digital signal in the low-voltage mixed signal process, the amplified signal having a high 4-wire echo return loss.

22. The method according to claim 21 further comprising the step of digitally filtering in the low-voltage mixed signal process, the digital signal converted from the amplified signal having a high 4-wire echo return loss.

23. The method according to claim 22 further comprising the step of communicating to a host processor, the digitally filtered signal converted from the amplified signal having a high 4-wire echo return loss.

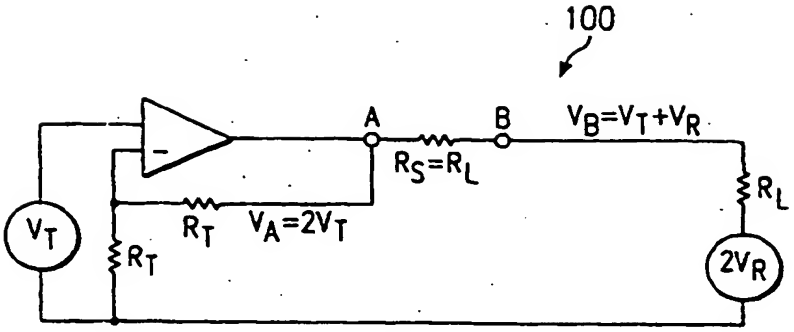


FIG. 1

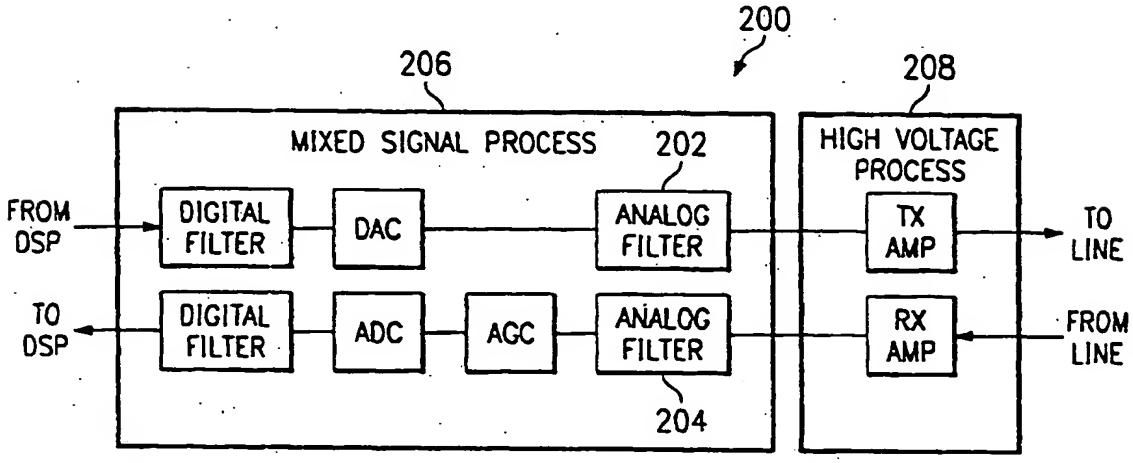


FIG. 2

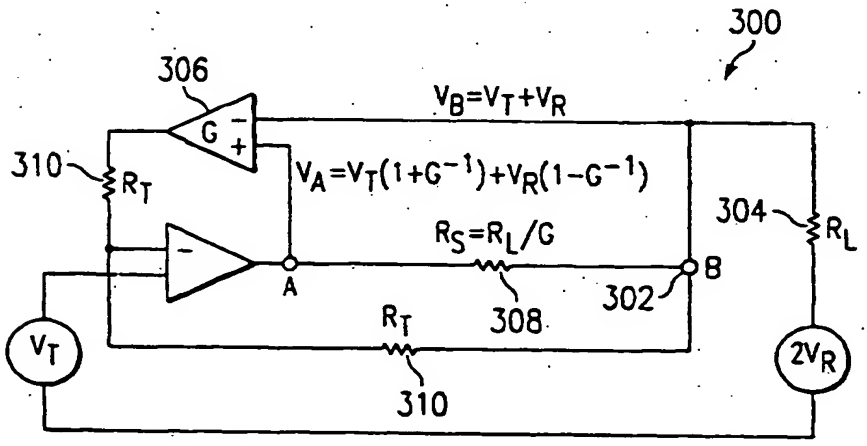


FIG. 3

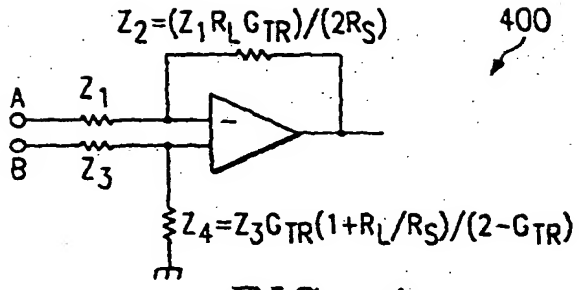

$Z_2=(Z_1R_LG_{TR})/(2R_S)$
400
A
B
Z_1
Z_3
$Z_4=Z_3G_{TR}(1+R_L/R_S)/(2-G_{TR})$

FIG. 4

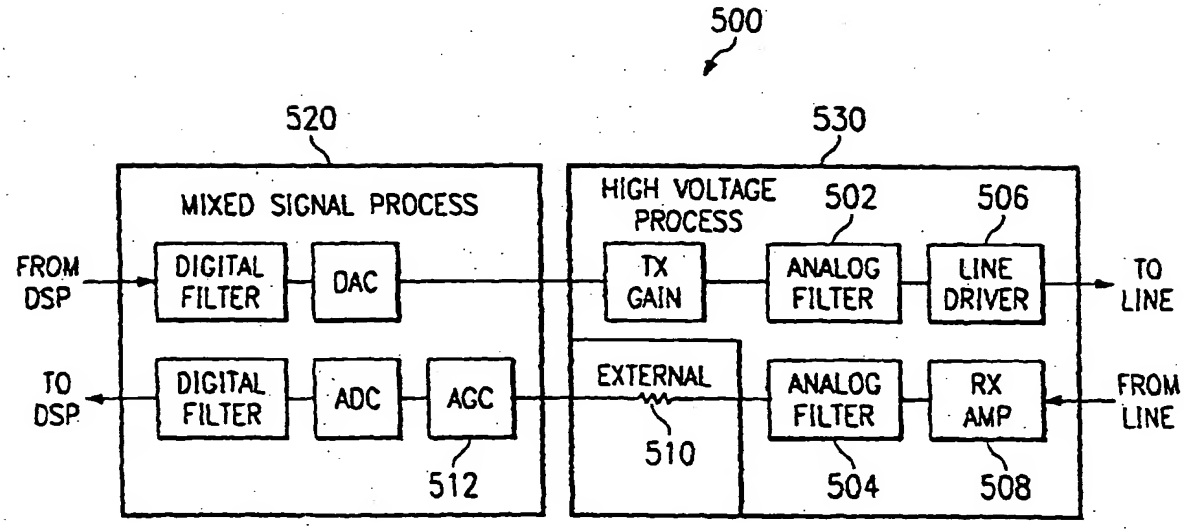
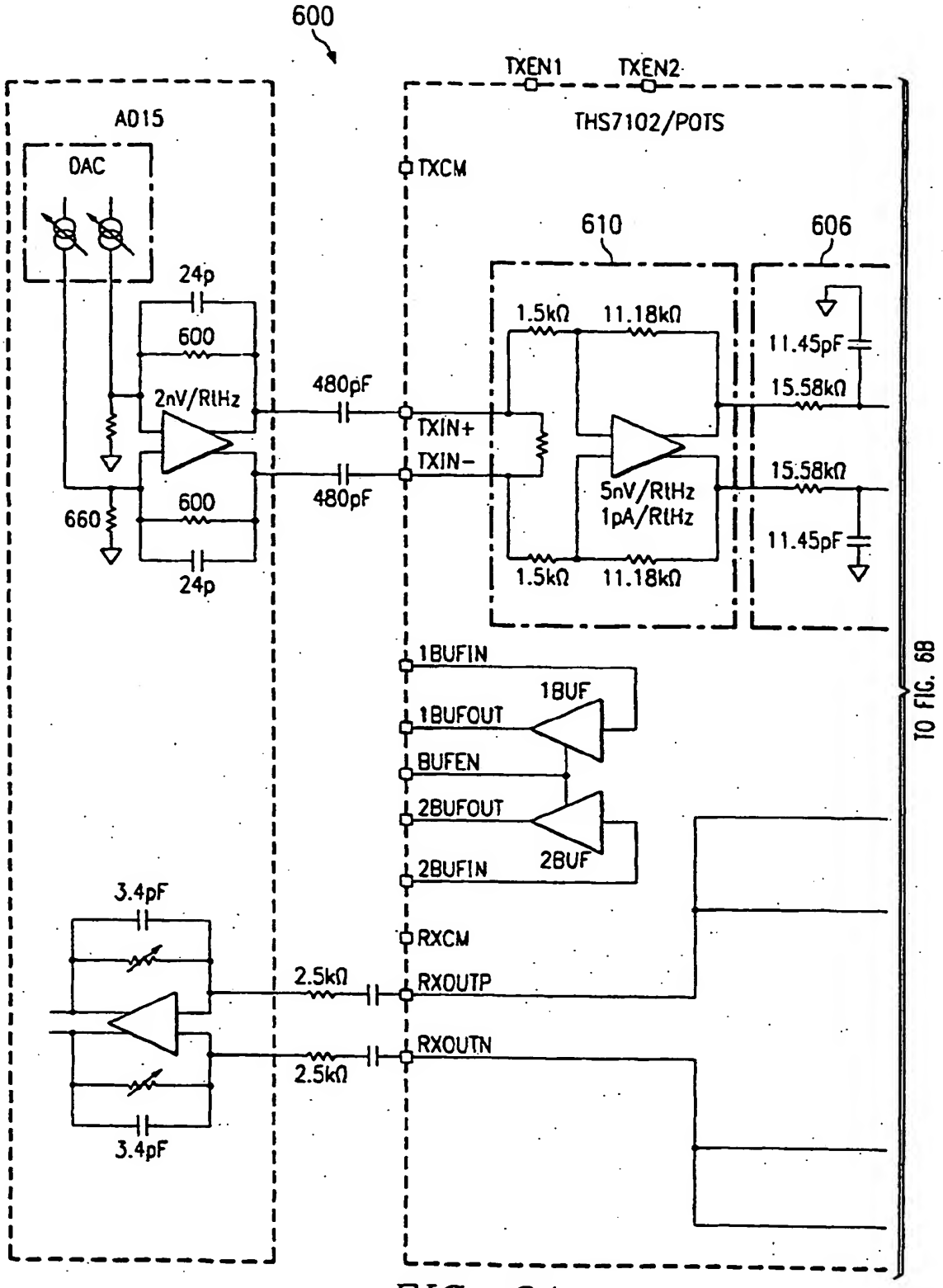

500
520
530
MIXED SIGNAL PROCESS
HIGH VOLTAGE PROCESS
502
506
FROM DSP
DIGITAL FILTER
DAC
TX GAIN
ANALOG FILTER
LINE DRIVER
TO LINE
TO DSP
DIGITAL FILTER
ADC
AGC
EXTERNAL
ANALOG FILTER
RX AMP
FROM LINE
510
512
504
508

FIG. 5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TXEN1
TXEN2
AD15
THS7102/POTS
DAC
TXCM
610
606
24p
600
2nV/RtHz
480pF
TXIN+
TXIN-
1.5kΩ
11.18kΩ
11.45pF
15.58kΩ
660
600
24p
480pF
5nV/RtHz
1pA/RtHz
1BUFIN
1BUF
1BUFOUT
BUFEN
2BUFOUT
2BUF
2BUFIN
3.4pF
RXCM
2.5kΩ
RXOUTP
RXOUTN
2.5kΩ
3.4pF
TO FIG. 6B

FIG. 6A

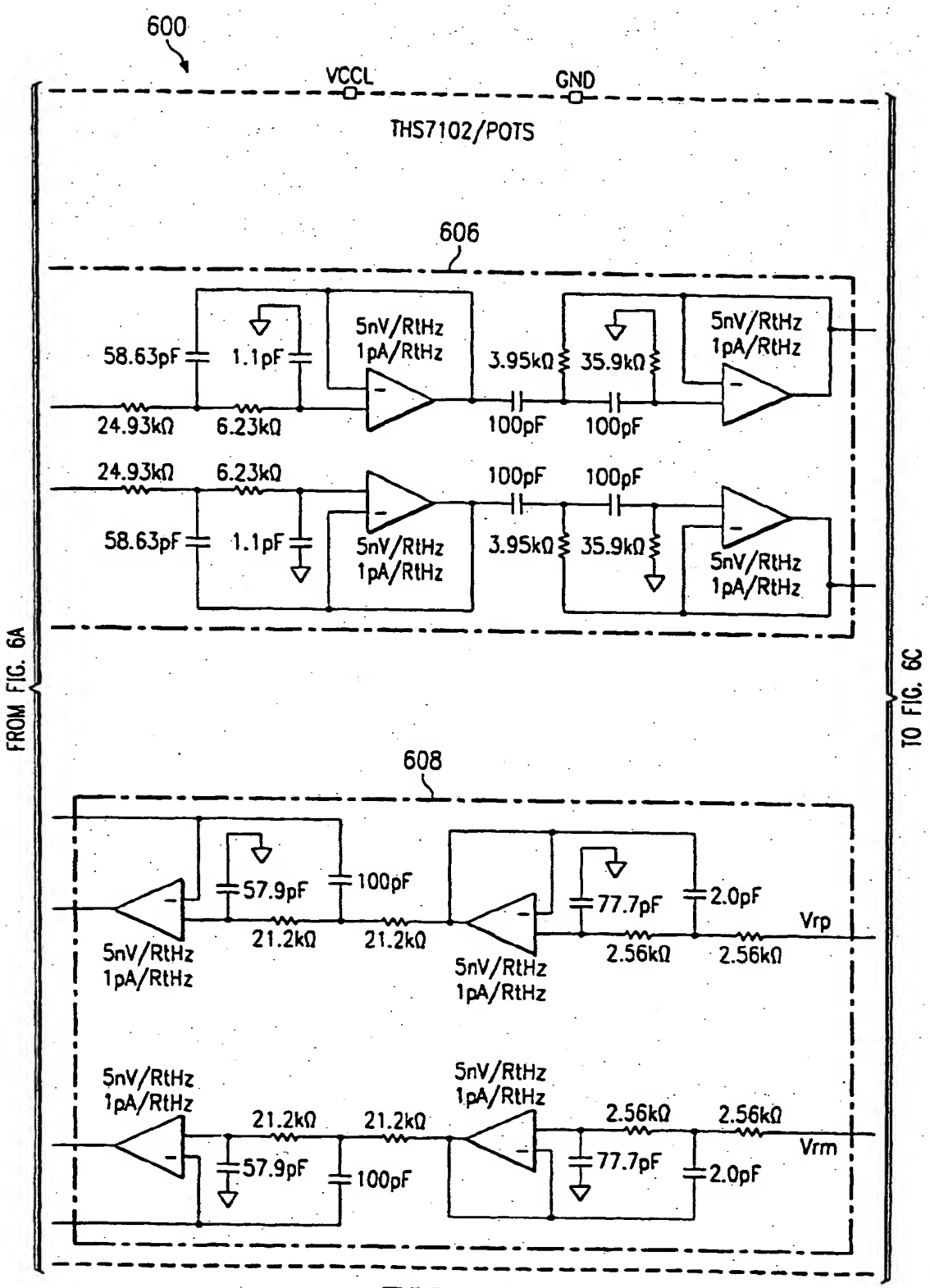
600
VCCL
GND
THS7102/POTS
606
58.63pF
1.1pF
5nV/RtHz
1pA/RtHz
3.95kΩ
35.9kΩ
5nV/RtHz
1pA/RtHz
24.93kΩ
6.23kΩ
100pF
100pF
24.93kΩ
6.23kΩ
100pF
100pF
58.63pF
1.1pF
5nV/RtHz
1pA/RtHz
3.95kΩ
35.9kΩ
5nV/RtHz
1pA/RtHz
FROM FIG. 6A
TO FIG. 6C
608
57.9pF
100pF
5nV/RtHz
1pA/RtHz
21.2kΩ
21.2kΩ
77.7pF
2.0pF
Vrp
5nV/RtHz
1pA/RtHz
2.56kΩ
2.56kΩ
5nV/RtHz
1pA/RtHz
5nV/RtHz
1pA/RtHz
21.2kΩ
21.2kΩ
2.56kΩ
2.56kΩ
Vrm
57.9pF
100pF
77.7pF
2.0pF

FIG. 6B

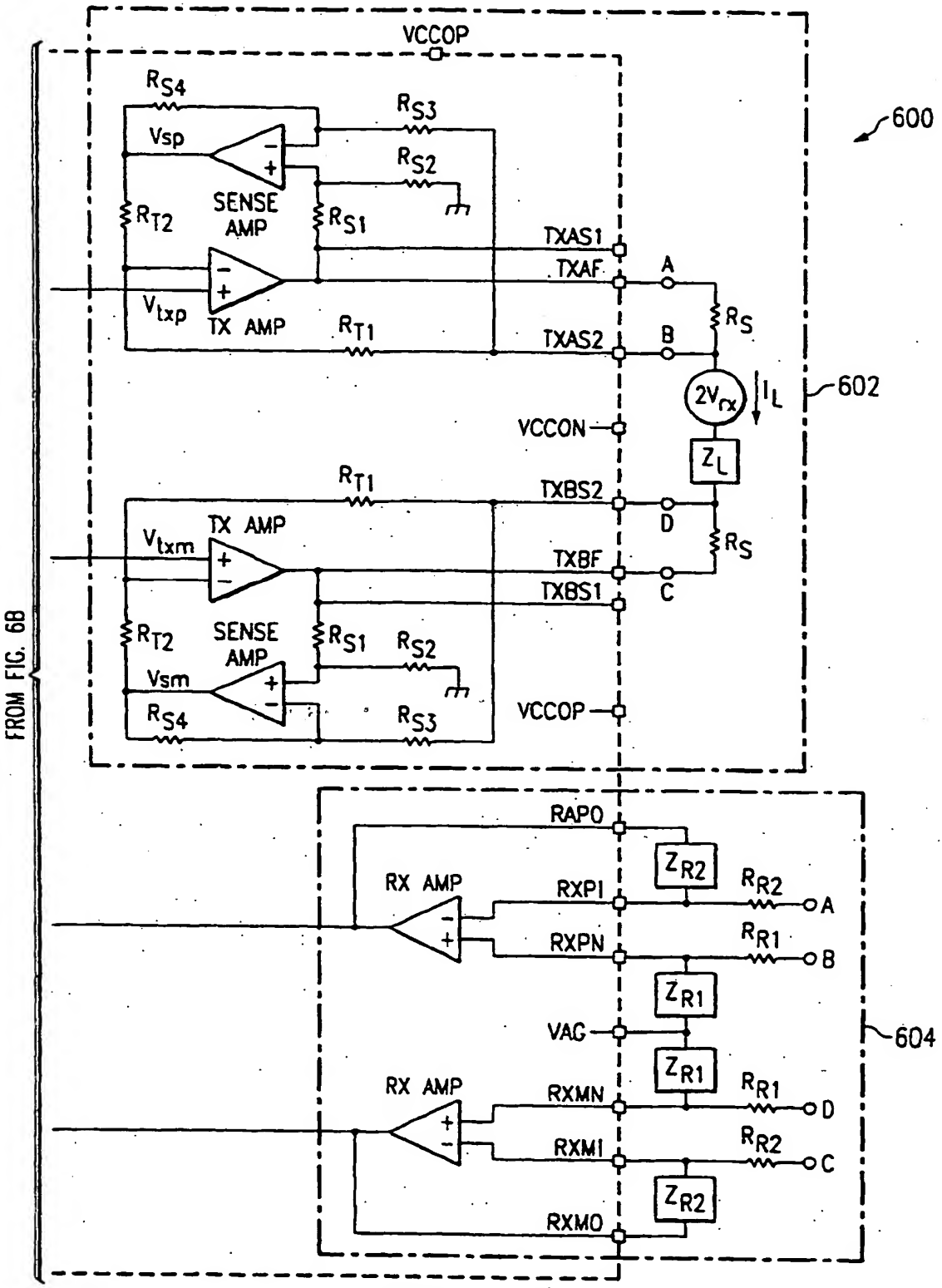
VCCOP
600
R_{S4}
R_{S3}
Vsp
R_{S2}
SENSE AMP
R_{T2}
R_{S1}
TXAS1
TXAF
A
V_{txp}
TX AMP
R_{T1}
TXAS2
B
R_S
$2V_{rx}$
I_L
602
VCCON
Z_L
R_{T1}
TXBS2
D
TX AMP
V_{txm}
R_S
TXBF
TXBS1
C
R_{T2}
SENSE AMP
R_{S1}
R_{S2}
Vsm
R_{S4}
R_{S3}
VCCOP
FROM FIG. 6B
RAPO
Z_{R2}
RX AMP
RXPI
R_{R2}
A
RXPN
R_{R1}
B
Z_{R1}
VAG
604
Z_{R1}
RX AMP
RXMN
R_{R1}
D
RXMI
R_{R2}
C
Z_{R2}
RXMO

FIG. 6C

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